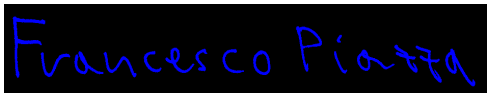
Qualification of the Saphyrion's SY1007S device

SY1007S Detail Specification

Saphyrion Designation: **SY1007S**

Manufacturer Cross Reference: **----**

Manufacturer: **Saphyrion Sagl**

Signature Field				
Prepared by	*F. Piazza* 		***Date***	*08 May 2017*
Approved by	*A. Consoli* 		***Date***	*08 May 2017*

CHANGE RECORD

Issue/ Revision	Date	Page	Description of Changes (see Section 3)
1-A	18.07.2007	all	Document creation.
1-B	18.08.2007	all	Document extended.
1-C	25.10.2007	all	Document extended.
1-D	21.11.2007	all	Document updated and extended.
1-E	30.11.2007	all	Document updated and extended.
1-F	10.12.2007	all	Document updated and extended.
1-G	23.09.2008	all	Document updated and extended to be consistent with the values in the test specification.
1-H	23.03.2009	all	Document updated and extended.
1-I	02.06.2009	all	Changed from Nemerix to Saphyrion.
1-L	01.09.2009	all	Updated limits to end of life expected values.
1-M	17.03.2012	all	Updated all sections, changed document format.
1-N	04.04.2012	all	Small refinements.
1-O	20.05.2012	all	Small refinements.
1-P	13.08.2012	all	Small refinements based on July 2012 review.
1-Q	21.09.2012	all	Small refinements based on August 2012 reviews.
1-R	08.02.2013	all	Small refinements based on February 2013 review.
1-S	12.02.2013	all	Small refinements based on February 2013 review.
1-T	18.02.2013	all	Small modifications according to 14th February 2013 e-mail (YZ).
1-U	06.03.2013	17-20	Corrected typos in figures 2.1 and 2.2 and in Table 2.4.
1-V	12.03.2013	1	Updated signature field on front page.
1-W	08.05.2015	all	Re-characterization of the SY1007, updated all sections and tables.
1-X	03.05.2017	7,10,11, 21,22	Minor update to pin naming (Section 1.10), added notes 9 and 10 (Table 14 in Section 2.6), added Section 3.

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1 GENERAL

1.1 Scope

This specification details the ratings, physical and electrical characteristics and test and inspection data for the SY1007S GNSS Receiver RF Front-End IC processed on Si/Ge technology. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification 9000.

1.2 Applicable Documents

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 Reference Documents

RD	Title	Version	Date
1	Saphyrion Sagl *SY1007 GNSS RF Front-End Datasheet*	1.4	31.01.2014
2	Saphyrion Sagl *SY1007 Test Specification*	3.4	13.09.2012
3	Micross (TS2-micro) *Process Identification Document - PID106*	6	26.06.2012
4	Optocap *Process Identification Document*		26.06.2012
5	Saphyrion Sagl *G3 ASIC Lot Validation 2 SY1007S Drift Analysis Report*	1-B	14.01.2013

Table 1: Reference documents.

1.4 Terms, Definitions, Abbreviations, Symbols and Units

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.5 Component Number and Component Type Variants

1.5.1 Component Number

The component type number shall be constituted as follows:

SY1007S

1.5.2 Marking

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall as a minimum be:

(a) Terminal identification.

(b) Component number.

(c) Traceability information.

← A1 dot and die part number: 07=SY1007.
← YYWW = Year and week of sealing.
← S = FM part, xxx = Unique serial number.

Marking	Meaning
Dot	Pin A1 position
07	Part number: SY1007
YYWW	Year and week of sealing
S	FM part
xxx	Unique serial number

Table 2: Marking on chip and meaning.

1.5.3 Component Type Variants

The component type variants applicable to this specification are as follows.

Variant number	Based on type	Circuit function	Analogue supply voltage	Digital supply voltage	Case	Terminal material and finish	Weight max
01	SY1007S	GNSS Receiver RF Front End	2.4V to 3.6V	2.2V to 3.6V	BGA-36	60/40 SnPb solder balls over Ni/Au plating	0.2g

Table 3: Component type variants.

Notes:

- Nickel: 2µm < Ni thickness < 8µm.
- Gold: Au is removed before ball attachment.

1.6 Absolute Maximum Ratings

Absolute maximum ratings are short term stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions are not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Characteristic	Symbol	Maximum rating	Unit	Notes
Positive analogue supply voltage	AVDD	4.0	V	1
Positive digital supply voltage	DVDD	4.0	V	1
ESD susceptibility, HBM, JESD22-A114	V(HBM)	Class 1B, 1	kV	
RF Input power, pins LNI and RFP/RFN	Pin	+10	dBm	
Continuous power dissipation	Pd	300	mW	2
Current in any pin	Imax	±1	mA	3
VB current	I(VB)	±50	mA	
VBG current	I(VBG)	±10	mA	
Voltage on any pin except LNI, RFP/RFN	Vmax	-0.3 / xVDD+0.3	V	4
RFN/RFP voltage	V(RFx)	0.9 to 1.5	V	5
LNI voltage	V(LNI)	±0.3	V	6
Operating junction temperature, guaranteed performance	Top	-40 to +125	°C	7
Operating junction temperature, no degradation	Tnd	-55 to +125	°C	8
Storage temperature	Tst	-65 to +150	°C	
Soldering temperature	Tsol	240	°C	9

Table 4: Absolute maximum ratings.

Notes:

1. From AVDD to AVSS, from DVDD to DVSS. MAX DC voltage between AVSS and DVSS ≤ ±100mV.
2. Provided maximum junction temperature is not exceeded.
3. Any pin except LNI, RFP/RFN, VB, VBG and power supply.
4. Any pin except LNI, RFP/RFN and power supply, provided other maximum ratings are not exceeded.
5. Shall be AC coupled. Do not force, shorting RFP/RFN to VSS will damage the device.
6. LNA shall be AC coupled when in use. Setting LNI to 0V disables the LNA.
7. With specified performance.
8. Functional performance is not guaranteed outside $T_{op.}$
9. Duration 40 seconds maximum.

1.7 Handling Precautions

ESD sensitive devices: these devices are susceptible to damage by electrostatic discharge, therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling.

These components are categorized as Class 1B with a minimum critical path failure voltage of 1000V HBM when tested in accordance with JEDEC JESD22-A114.

1.8 Functional Description

The SY1007S is a radiation hardened L-band RF down-converter for GNSS receivers aimed at the space market. This device includes all functional blocks needed to implement a complete super-heterodyne RF front-end for multi-band GNSS receivers, thus allowing a substantial reduction of BOM, size and weight with respect to discrete designs. It directly interfaces to the ESA AGGA-4 GNSS base-band processor.

The SY1007S is implemented in a 0.35µm SiGe HBT process and comes in a ceramic-metal hermetic 36 balls CBGA package containing no organic materials, while eutectic – rather than epoxy – die attach has been used. This device will therefore not decompose or release any substantial amount of gas or organic contaminants under vacuum or high radiation levels.

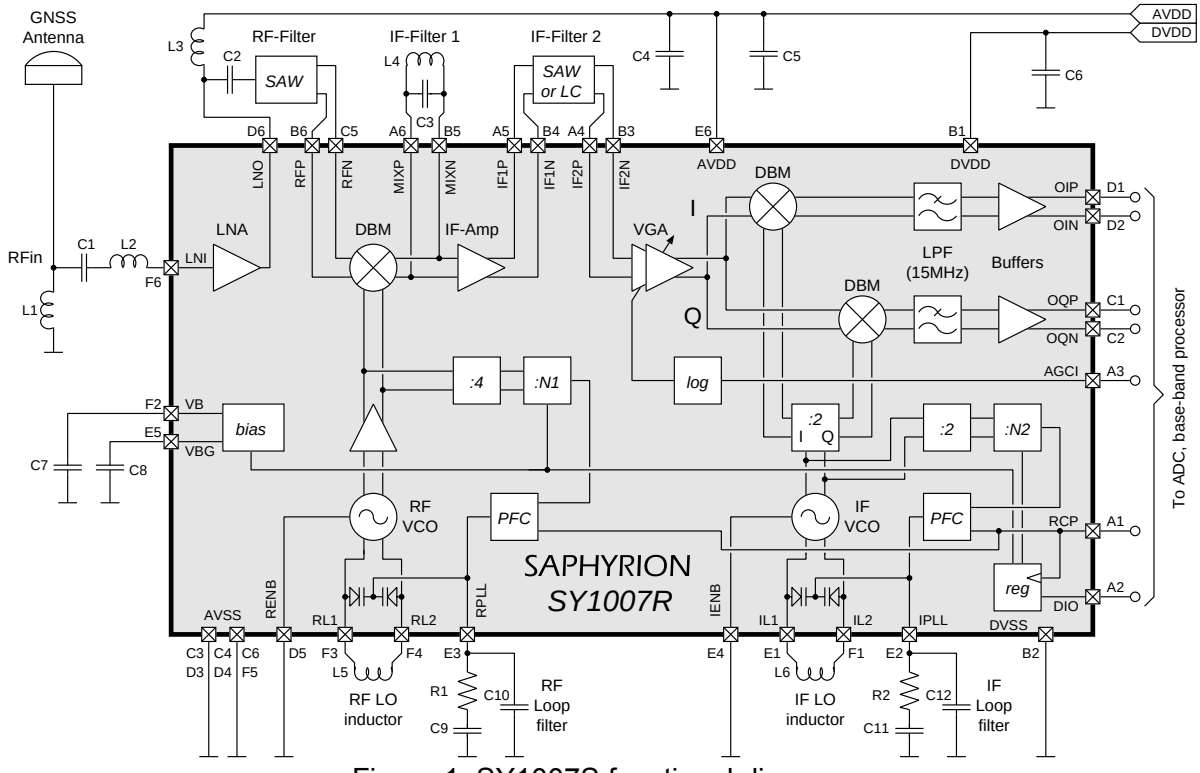

Figure 1: SY1007S functional diagram.

1.9 Physical Dimensions

The CBGA package of the SY1007S is of ceramic-metal hermetic design, similar in shape to a plastic BGA, JEDEC MO-216, variant BAA-2 (thickness is larger). Connection to the PCB is via solder balls, which result in a rather rigid assembly.

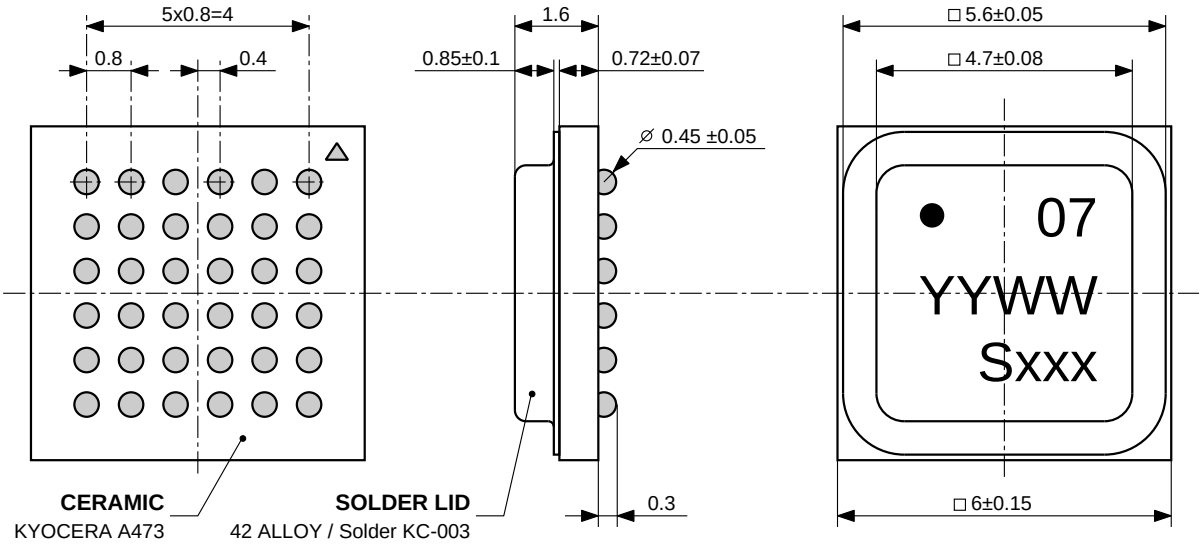

Figure 2: SY1007S mechanical drawing (CBGA 36 balls).

1.10 Pin Identification

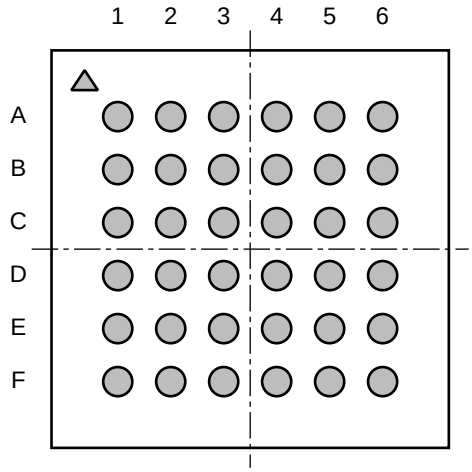

Figure 3: SY1007S pin-out (top view).

1.11 Pin Description

Name	Ball	Function	Notes
A-balls			
RCP	A1	External reference clock input.	
DIO	A2	Data input/output. Test: scan output.	Needs a weak pull down.
AGCI	A3	IF VCA gain control voltage input.	Decouple to AVSS close to pin.
IF2P	A4	IF VGA positive input.	
IF1P	A5	First IF amplifier positive output.	
MIXP	A6	RF mixer's positive IF output.	
B-balls			
DVDD	B1	Positive digital supply voltage.	
DVSS	B2	Negative digital supply voltage.	
IF2N	B3	IF VCA negative input.	
IF1N	B4	First IF amplifier negative output.	
MIXN	B5	RF mixer's negative IF output.	
RFP	B6	RF mixer's positive RF input.	Shall be AC-coupled, do not force.
C-balls			
OQP	C1	Quadrature near baseband positive output.	Load shall be ≥10kΩ.
OQN	C2	Quadrature near baseband negative output.	Load shall be ≥10kΩ.
AVSS	C3	Negative analogue supply voltage.	
AVSS	C4	Negative analogue supply voltage.	
RFN	C5	RF mixer's negative RF input.	Shall be AC-coupled, do not force.
AVSS	C6	Negative analogue supply voltage.	
D-balls			
OIP	D1	In-phase near baseband positive output.	Load shall be ≥10kΩ.
OIN	D2	In-phase near baseband negative output.	Load shall be ≥10kΩ.
AVSS	D3	Negative analogue supply voltage.	
AVSS	D4	Negative analogue supply voltage.	
RENB	D5	RF PLL enable – active low. Test: scan enable.	
LNO	D6	Output of the LNA.	Requires matching network.
E-balls			
IL1	E1	IF VCO tank-circuit's inductor – first terminal.	
IPLL	E2	IF PLL phase-frequency comparator's output.	Connect to IF loop filter.
RPLL	E3	RF PLL phase-frequency comparator's output.	Connect to RF loop filter.
IENB	E4	IF PLL Enable – active low. Test: scan input.	
VBG	E5	Band-gap voltage reference output, 1.2V.	Decouple to AVSS close to pin.
AVDD	E6	Positive analogue supply voltage.	
F-balls			
IL2	F1	IF VCO tank-circuit's inductor – second terminal.	
VB	F2	Voltage regulator's output, 1.9V.	Decouple to AVSS close to pin.
RL1	F3	RF VCO tank-circuit's inductor – first terminal.	
RL2	F4	RF VCO tank-circuit's inductor – second terminal.	
AVSS	F5	Negative analogue supply voltage.	
LNI	F6	Input of the LNA. Connect to VSS to disable LNA.	Requires matching network.

Table 5: Pin-out list.

1.12 Timing Diagram, Data Structure and Register Map

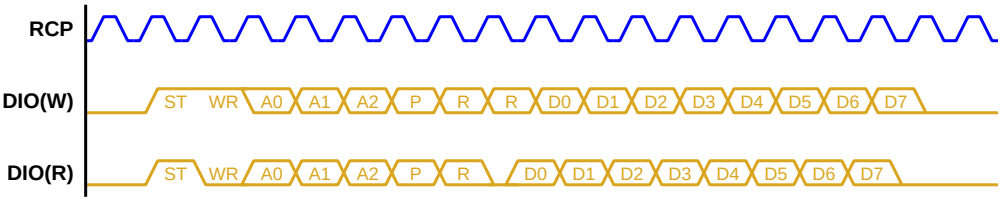

Figure 4: Interface timing.

Field name	Start Bit	Write	Addr [0:2]	Parity	Reserved	Data [0:7]
Position	0	1	2:4	5	6(7)	8:15

Table 6: Data structure.

Field Name	**Description**
Start bit	Must go HIGH to start communication.
Write	Transfer direction: 0 = READ operation, 1 = WRITE operation.
Addr [0:2]	Register address, LSB first (A0 is the LSB, see Table 8).
Parity	Parity is calculated on Start bit, Write and Address fields. Parity is ODD, i.e. the number of 1s in bits [5:0] of the control word must be odd.
Reserved	Reserved, currently not used (1 bit for read, 2 bits for write).
Data [0:7]	- *Write operation:* the master sends the data to be written into a register of the SY1007. - *Read operation:* the SY1007 returns the register's content. - Data is LSB-first (Data[0] is the LSB).

Table 7: Data structure details.

Register address			**Register Name**
A0	**A1**	**A2**	
0	0	0	RF-PLL
0	0	1	(Reserved)
0	1	0	Power Modes
0	1	1	(Reserved)
1	0	0	IF-PLL
1	0	1	(Reserved)
1	1	0	(Reserved)
1	1	1	(Reserved)

Table 8: Register's map.

1.13 ESD Protection Networks

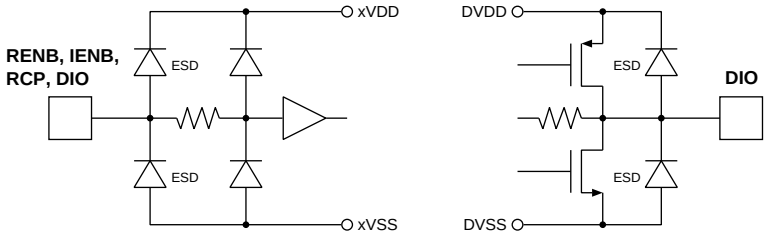

Figure 5: Digital inputs and outputs.

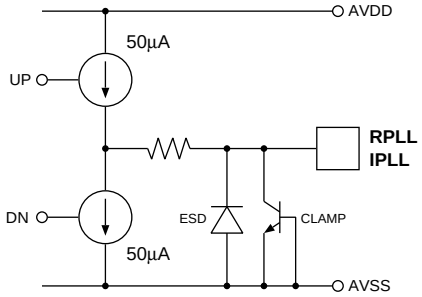

Figure 6: PLL charge pump outputs.

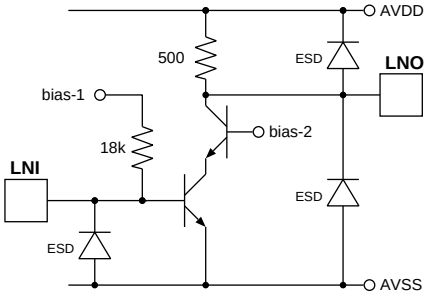

Figure 7: LNA input and output.

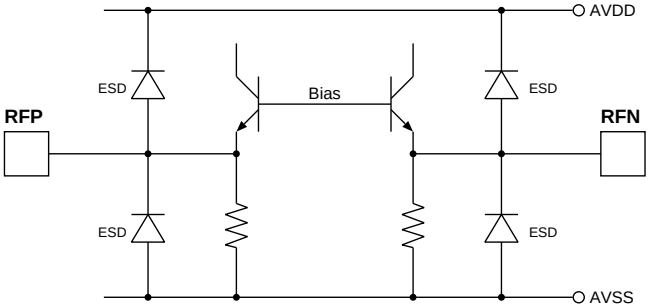

Figure 8: RF mixer's input.

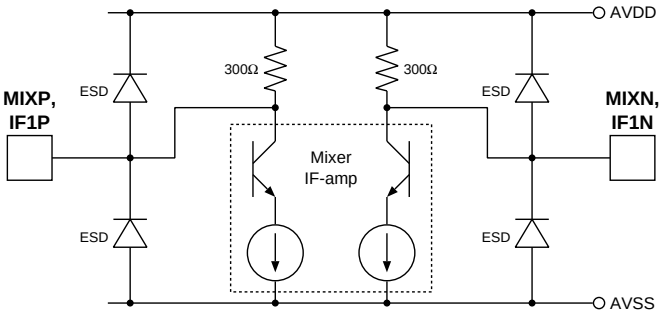

Figure 9: IF input/output (mixer, IF-amplifier).

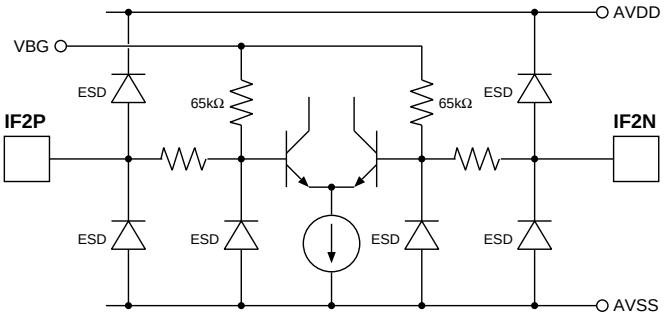

Figure 10: IF VCA input (AGC).

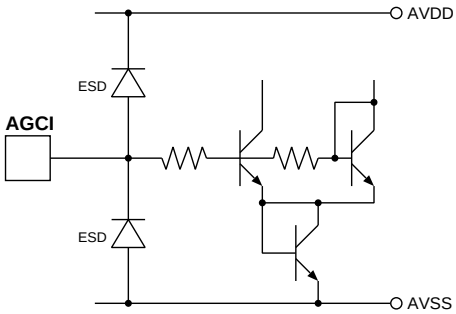

Figure 11: PGA gain control input.

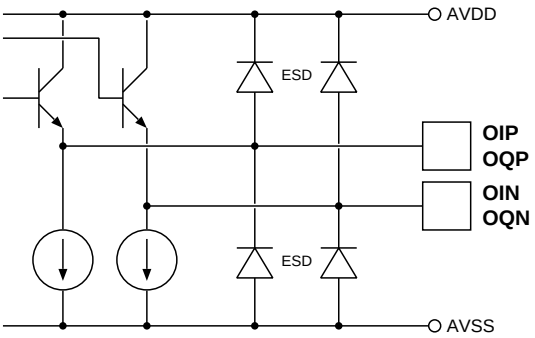

Figure 12: I/Q near baseband outputs.

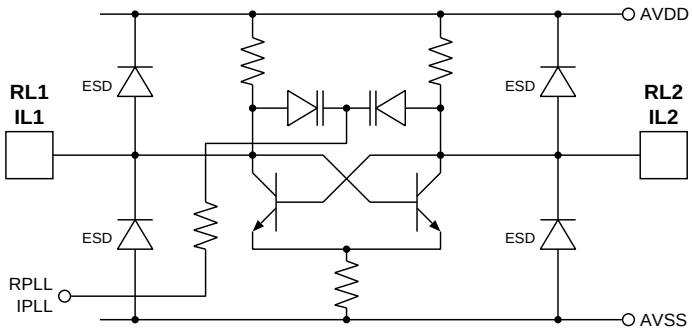

Figure 13: RF and IF voltage controlled oscillators.

2 REQUIREMENTS

2.1 General

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are as listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from Screening Tests – Chart F3.

High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB Burn-in shall be omitted.

2.2 Wafer Manufacturing & Preparation

For 3 wafers B4681 manufactured at AMS the wafer lot acceptance data are prepared according to ESCC9000 Chart F2 – Production Control – Wafer Lot Acceptance. The Wafer Lot Acceptance data consists of the Process Monitoring Review supported by the Process Identification Document (PID), the SEM Inspection and the Total Dose Radiation Testing (TID). During the development of the SY1007S TID and Single Event Effects (SEE) testing have been performed, only the TID testing is repeated for the flight wafer.

Test type	**Specification**	**SY1007S**
Process Monitoring Review	ESCC9000, Chart F2	
SEM Inspection	ESCC9000, Chart F2	4 pieces per wafer
TID Testing	ESCC9000, Chart F2	4 pieces

Table 9: Wafer lot acceptance.

2.3 Production of Flight Lot

During this activity the parts for the flight lot are packaged according to ESCC9000 Chart F2 – Production Control – Special In-Process Controls.

The following steps are performed:

- Die assembly.
- Pre-cap inspection.
- Sealing.
- Marking of the devices.
- Balling.

Test type	**Specification**	**SY1007S**
Internal visual inspection	ESCC9000, Chart F2	All
Pre-cap inspection • Low magnification • High magnification	ESCC9000, Chart F2	 All 50 pieces
Bond strength at pre-cap	ESCC9000, Chart F2	3 pieces
Die shear at pre-cap	ESCC9000, Chart F2	3 pieces
External dimension check at pre-cap	ESCC9000, Chart F2	3 pieces
Co-planarity of solder balls	ESCC9000, Chart F2 Co-planarity (CO) < 120µm	All

Table 10: Special in-process controls.

2.4 Screening of Flight Lot

During this activity the parts for the flight lot are screened according to ESCC9000 Chart F3 (Figure 14). The tests are given in Table 11.

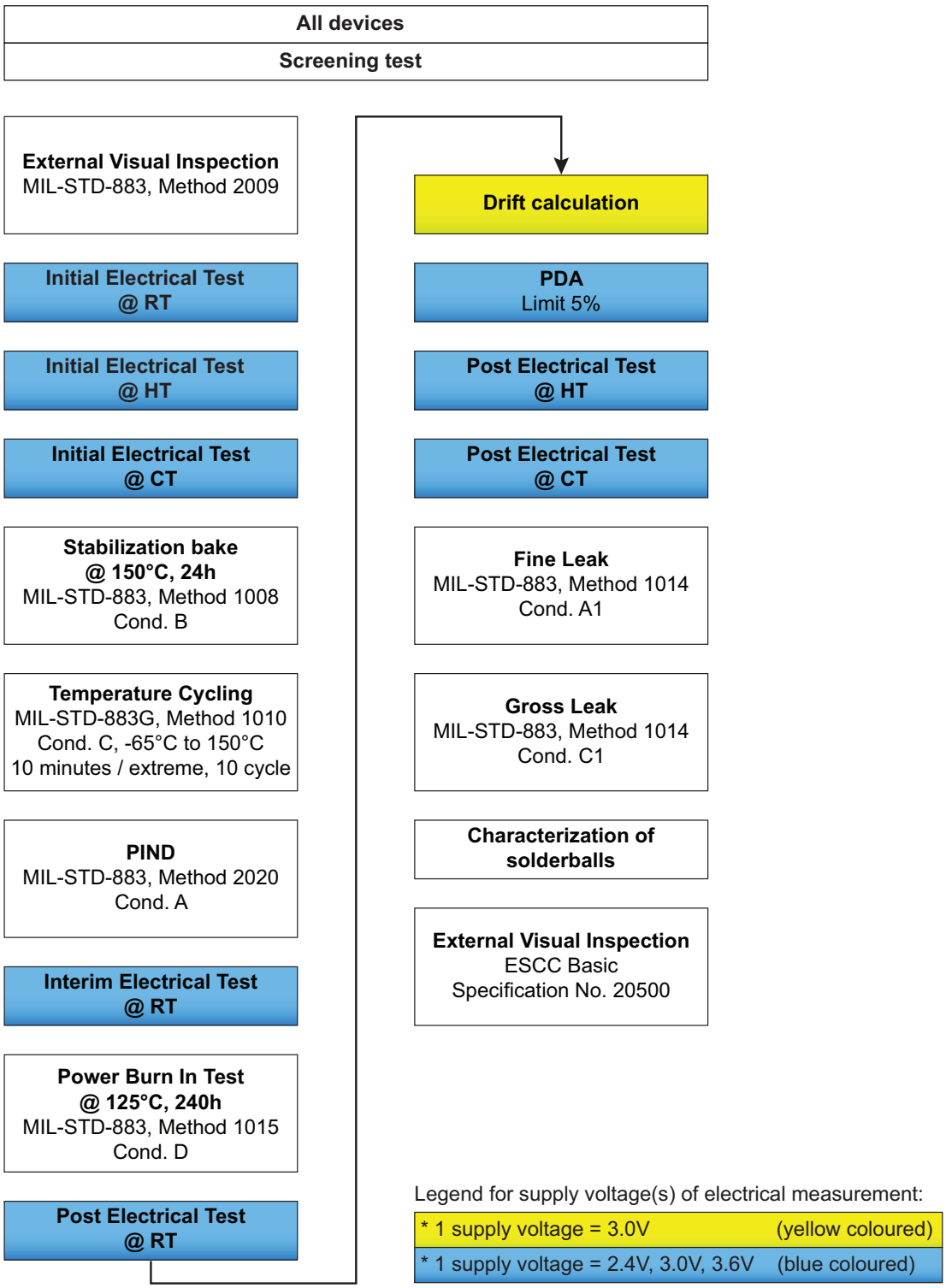

Figure 14: Screening tests flow chart – Chart F3.

Test type	**Specification**	**SY1007S**
Initial electrical test room temperature.	ESCC9000, Chart F3 SY1007S-Test Spec, chapter 6	All
Initial electrical test high temperature.	ESCC9000, Chart F3 SY1007S-Test Spec, chapter 6	All
Initial electrical test cold temperature.	ESCC9000, Chart F3 SY1007S-Test Spec, chapter 6	All
150°C temperature stabilization bake for 24h.	ESCC9000, Chart F3	All
Temperature cycling form -65°C to 150°C, 10 minutes for 10 cycles.	ESCC9000, Chart F3	All
Particle impact noise detection (PIND).	ESCC9000, Chart F3	All
Interim electrical measurements, at room temperature.	ESCC9000, Chart F3 SY1007S-Test Spec, chapter 7	All
Power burn-in under nitrogen atmosphere.	ESCC9000, Chart F3	All
Post electrical measurements, at room temperature.	ESCC9000, Chart F3 SY1007S-Test Spec, chapter 7	All
Drift calculation.	ESCC9000, Chart F3 SY1007S-Test Spec, chapter 7	
PDA limits (5%).		
Characterization of solder balls (optical, co-planarity).	ESCC9000, Chart F3, **note 1**	All
Seal (fine and gross leak).	ESCC9000, Chart F3	All
External visual inspection.	ESCC9000, Chart F3	All
Check for lot failure.	ESCC9000, Chart F3	All

Table 11: Screening tests.

Notes:

1. Visual inspection of solder balls. Criteria: no missing balls, no missing material of the surface and co-planarity shall be less than 0.12 mm (120µm).

2.5 Lot Validation of Flight Lot

During this activity a set of reliability tests are performed on the packaged parts. The test and the number of samples are given in Table 12 whereas the test flow is provided in Figure 15.

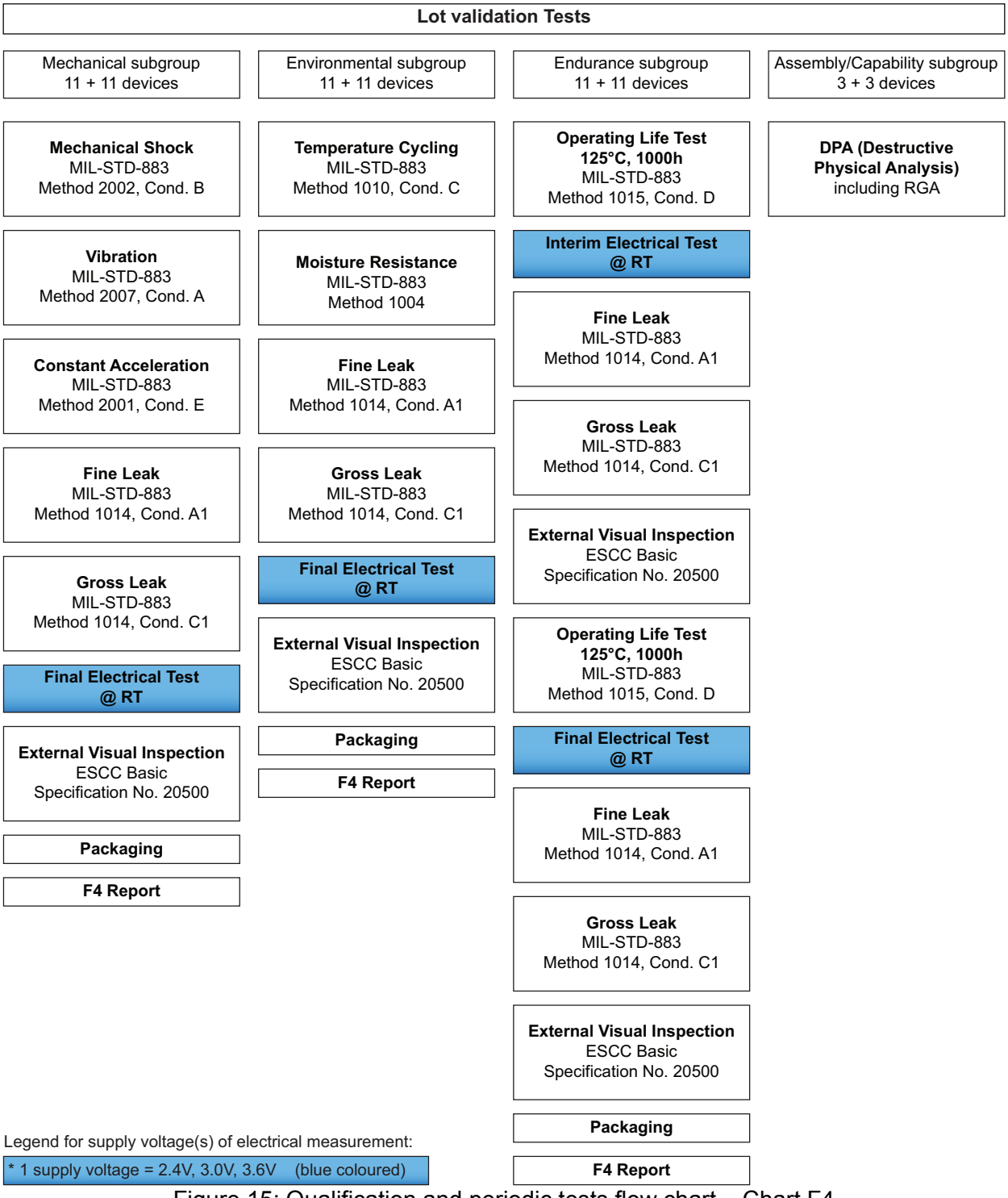

Figure 15: Qualification and periodic tests flow chart – Chart F4.

Test Type	**Specification**	**SY1007S**
Solderability	TP-PLN-0036-AAE_1	5 pieces
F4-Qualification Tests – Mechanical Subgroup		11 pieces
Mechanical shock	ESCC9000, Chart F4, Subgroup 1	11 pieces
Vibration	ESCC9000, Chart F4, Subgroup 1	11 pieces
Constant acceleration	ESCC9000, Chart F4, Subgroup 1	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
Final electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 1 SY1007S-Test Spec, chapter 7	11 pieces
F4-Qualification Tests – Environmental Subgroup		11 pieces
Temperature cycling (10 cycles)	ESCC9000, Chart F4, **note 1**	11 pieces
Moisture resistance	ESCC9000, Chart F4, Subgroup 1	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
Final electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 1 SY1007S-Test Spec, chapter 7	11 pieces
F4-Qualification Tests – Endurance Subgroup		11 pieces
Operating life test on qualification sample 1000h	ESCC9000, Chart F4, Subgroup 2	11 pieces
Interim electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 2 SY1007S-Test Spec, chapter 7	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
External visual inspection	ESCC9000, Chart F4, Subgroup 1	11 pieces
Operating life test on qualification sample 1000h	ESCC9000, Chart F4, Subgroup 2	11 pieces
Final electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 2 SY1007S-Test Spec, chapter 7	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
External visual inspection	ESCC9000, Chart F4, Subgroup 1	11 pieces
F4-Qualification Tests – Assembly/Capability Subgroup		3 pieces
External visual inspection	ESA/SCC Basic Specification No. 2059000, Issue 1, September 1994.	3 pieces
Radiographic inspection	ESA/SCC Basic Specification No. 2099000, Issue 1, September 1994.	3 pieces
PIND test	MIL-STD-883, Method 2020, Cond. A.	3 pieces
Hermetic seal tests	MIL-STD-883, Method 1014, Cond. A1 and C1.	3 pieces
Internal gas analysis	MIL-STD-883, Method 1018.	3 pieces
Internal visual inspection	ESCC Basic Specification No. 2049000, Issue 2, November 2003.	3 pieces
Bond strength	MIL-STD-883, Method 2011.	3 pieces

Table 12: Lot validation tests and number of samples.

Notes:

1. The temperature cycling (MIL-STD-883, Method 1010, Condition C) present in the test flow is defined in the ESCC9000, issue 1 (October 2002) and older versions as part of the flow. At the time of the qualification of the lot 1 this was the version in use and temperature cycling was agreed with ESA and RUAG as enough. Because of that, the thermal shock was not implemented as part of the flow.

2.6 Electrical Measurements at Room, High and Low Temperatures

For typical performances, operating characteristics, circuit description and applications notes please refer to the data sheet [RD1]. *Saphyrion Sagl reserves the right to change the detail specifications as may be required to permit improvements in the design of its products* (wording according to JEDEC JEP103A).

2.6.1 Functional Tests Dependent on Temperature

Conditions: AVDD = 2.4V to 3.6V, DVDD = 2.2V to AVDD+0.2V, f(RCP) = 2.0MHz, Tjunction = −40°C to +125°C, no load, unless otherwise stated. All voltages are referred to their respective VSS. Typical values are at AVDD = 3.0V, DVDD = 3.0V, Tjunction = +25°C.

Characteristics	Symbol	Test conditions	Limits		Units	Ref. to [RD2] section	Notes
			Min	Max			
Analogue supply current @−40$^{+5}/_{-0}$°C	I_{SSA-40}	Sleep	0.0	5.0	µA	6.4.1	1
		Doze	180.0	345.0	µA	6.4.2	1
		Stand-by	2.0	4.5	mA	6.4.3	1
		Active	9.5	13.5	mA	6.4.4	1
Analogue supply current @+25$^{+5}/_{-5}$°C	I_{SSA+25}	Sleep	0.0	5.0	µA	6.4.1	1
		Doze	180.0	360.0	µA	6.4.2	1
		Stand-by	2.5	5.0	mA	6.4.3	1
		Active	11.5	18.0	mA	6.4.4	1
Analogue supply current @+125$^{+0}/_{-5}$°C	$I_{SSA+125}$	Sleep	0.0	5.0	µA	6.4.1	1
		Doze	200.0	380.0	µA	6.4.2	1
		Stand-by	2.5	5.5	mA	6.4.3	1
		Active	12.5	19.0	mA	6.4.4	1

Table 13: Functional tests dependent on temperature.

2.6.2 Functional Tests Independent from Temperature

Conditions: AVDD = 2.4V to 3.6V, DVDD = 2.2V to AVDD+0.2V, f(RCP) = 2.0MHz, Tjunction = −40°C to +125°C, no load, unless otherwise stated. All voltages are referred to their respective VSS. Typical values are at AVDD = 3.0V, DVDD = 3.0V, Tjunction = +25°C.

Characteristics	Symbol	Test conditions	Limits		Unit	Ref. to [RD2]	Notes
			Min	Max			
Digital Section							
Digital supply current	I_{SSD}	Sleep	0.0	5.0	µA	6.4.1	1
		Doze	0.0	5.0	µA	6.4.2	1
		Stand-by	20	60	µA	6.4.3	1
		Active	20	60	µA	6.4.4	1
Digital output high level	V_{OH}	I_{OH} = −1mA	0.9 x DVDD		V	6.6.1	1
Digital output low level	V_{OL}	I_{OL} = 1mA		0.1 x DVDD	V	6.6.1	1
Digital output rise time	t_r	10 to 90%, C_{load} = 5pF		6.1	ns		2
Digital output fall time	t_f	90 to 10%, C_{load} = 5pF		4.8	ns		2
Band-gap reference and voltage regulator							
Band-gap reference voltage	V_{BG}	No load	1.11	1.18	V	6.5.2	1
Band-gap reference load regulation	ΔV_{BG} vs. ΔI_{BG}	I_{VBG} = 0 to −300µA	0	20.0	mV	6.5.2	1
				5.0	mV		4
Band-gap reference line regulation	ΔV_{BG} vs. Δ AVDD	AVDD = 2.4V to 3.6V		5	mV	6.5.2	1
Voltage regulator output voltage	V_B		1.75	1.95	V	6.5.2	1
Voltage regulator load regulation	ΔV_B	I_{VB} = 0 to −4mA	0	20	mV	6.5.2	1
				15	mV		4
Voltage regulator line regulation	ΔV_B vs. Δ AVDD	AVDD = 2.4 to 3.6V		10	mV	6.5.2	1
Voltage regulator output current	I_B		-4		mA	6.5.2	1
RF PLL frequency synthesizer							
RF PLL main divider range	M_{RF}		64	255		6.5.4	1
LO RF PLL VCO frequency range	RF_{freq}	L=4.7nH, see **note 9!**	1.35	1.50	GHz		3, 9
LO RF PLL VCO sensitivity	$Sens_{RF}$	L=4.7nH, see **note 9!**	740	1050	MHz/V	6.5.3	3, 9
LO RF PLL charge pump current	I_{CPRF}		42	63	µA		5
RF SSB phase noise PLL	φn	100Hz offset		−58	dBc/Hz		6, 8
		1kHz offset		−66	dBc/Hz		6, 8
		10kHz offset		−68	dBc/Hz		6, 8
		100kHz offset		−70	dBc/Hz		6, 8
		1MHz offset		−100	dBc/Hz		6, 8
RF PLL spurs		Recommended loop filter		−40	dBc		6, 8
External RF LO signal amplitude	V_{RFext}	Differential, RENB = 1	−17	+5	dBu	6.5.12	1
IF PLL frequency synthesizer							
IF PLL main divider range	M_{IF}		32	255		6.5.6	1
LO IF PLL VCO frequency range	IF_{freq}	L=47nH, see **note 9!**	360	420	MHz		3, 9
LO IF PLL VCO sensitivity	$Sens_{IF}$	L=47nH, see **note 9!**	160	298	MHz/V	6.5.5	3, 9
LO IF PLL charge pump current	I_{CPIF}		42	63	µA		5
IF SSB phase noise PLL	φn	100Hz offset		−78	dBc/Hz		6, 8
		1kHz offset		−86	dBc/Hz		6, 8
		10kHz offset		−88	dBc/Hz		6, 8
		100kHz offset		−95	dBc/Hz		6, 8
		1MHz offset		−110	dBc/Hz		6, 8
IF PLL spurs		Recommended loop filter		−60	dBc		6, 8
External IF LO signal amplitude	VI_{Fext}	Differential, IENB = 1	−17	+5	dBu	6.5.12	1
Low noise amplifier							
Voltage on LNA input	V(LNI)	LNA off	−3	+3	mV	6.5.7	1
		LNA on	0.45	0.83	V	6.5.7	1
LNA bias current	I (LNA)	LNA on	1.95	4.30	mA	6.5.7	1
LNA Gain	G_{LNA}	Power gain, noise matched	18.2	25.0	dB		5, 6
LNA noise figure	NF_{LNA}	Noise matched		1.8	dB		6, 8
LNA group delay	GD	Noise matched	1.19	1.29	ns		6, 8
LNA 1dB compression point	iCP_{LNA}	Input referred	−24	−20	dBm		6, 8
LNA 3rd order intercept point	iIP3	Input referred	−14		dBm		6, 8
LNA input reflection coefficient	S11	Noise matched		−2	dB		6, 8
LNA output reflection coefficient	S22	Z-matched		−15	dB		6, 8

Characteristics	Symbol	Test conditions	Limits		Unit	Ref. to [RD2]	Notes
			Min	Max			
RF mixer							
Voltage on mixer's RF input	V(RFx)	Mixer on	0.20	0.60	V	6.5.8	1
Voltage on mixer's IF output	V(MIXx)	Mixer off, AVDD = 3V	2.95	3.05	V	6.5.8	1
		Mixer on, AVDD = 3V	2.57	2.85	V	6.5.8	1
RF Mixer conversion gain	G_{Mixer}	Voltage gain, to IF1x.	24	29	dB	6.5.8	1, 7
RF Mixer SSB noise figure	NF_{Mixer}	Differential output.		13.5	dB		6, 8
RF Mixer 1dB compression point	iCP_{Mixer}	Input referred.	−16		dBm		6, 8
RF Mixer input refl. coefficient	S11	@1.57GHz.		−15	dB		6, 8
RF differential output resistance	R_{diffRF}	MIXP to MIXN	500	720	Ω	6.2	1
IF-strip and near base-band output							
Voltage on 1st IF output	V (IFx)	Mixer off AVDD = 3V	2.95	3.05	V	6.5.8	1
		Mixer on AVDD = 3V	2.78	2.90	V	6.5.8	1
IF differential output resistance	$R_{diffout}$	IF1P to IF1N	500	720	Ω	6.2	1
IF differential input resistance	R_{diffin}	IF2P to IF2N	54	81	kΩ	6.2	1
Voltage on 2nd IF input	V (IF2x)		1.10	1.18	V	6.5.9	1
AGC voltage gain	G_{AGC}	OI to IF2, $V_{AGC} \geq 2V$	64		dB	6.5.10	1,7
AGC control range	GC_{AGC}	$0.3 \leq V_{AGC} \leq 1.5V$	50		dB	6.5.10	1
AGC sensitivity	$Sens_{AGC}$		6	12	mV/dB	6.5.10	1
AGC control voltage, max gain	V_{AGCmax}			2	V	6.5.10	1
AGC control voltage, min gain	V_{AGCmin}		0.2		V	6.5.10	1
Output signal amplitude	V_{OUT}	≤ 1dB compression	1.5	2.1	V	6.5.9	1
DC offset voltage	V_{OS}	I/Q outputs, differential	−30	30	mV	6.5.9	1
I/Q output impedance	Z_{iq}	See **note 10!**	120	150	Ω		4, 8, 10
I/Q max load capacitance	C_{iq}	No bandwidth reduction		10	pF		4, 8
I/Q low-pass filter bandwidth	f(-3dB)	On-chip LPF.	12	18	MHz	6.5.11	1

Table 14: Functional tests independent from temperature.

Notes:

1. Fully tested over temperatures −40°C, 25°C, 125°C, and voltages 2.4V, 3.0V, 3.6V. Selected parameters are tested at limits different than shown in the data sheet, either to get margin (tighter limits) or to account for the non-ideal test system (looser limits). Current consumption in Sleep mode is masked by tester resolution and leakages. Typical current consumption in Sleep mode is <100nA on both AVDD and DVDD (also at 125°C).
2. As 1 but calculated from measurement at higher load capacitances (load board stray and tester input capacitance are >> 15pF).
3. As 1 but tested indirectly via PLL loop filter voltage measurements. VCOs are tested at lower frequencies against limits applicable to the actual test conditions and verified with KGDs. Load board stray inductance and capacitance prevent direct measurement.
4. Guaranteed by design only.
5. Guaranteed by design only. Functionally tested indirectly via loop filter measurements (Icp), verified by correlation with tests 6.5.7 (LNA) and 6.5.8 (Mixer).
6. On characterization test board (not load board) with proper alignment of all external components (matching networks, inductors, etc).
7. Losses (load board, matching network, socket, …) are compensated by setting signal power accordingly (using KGDs).
8. Not production tested, only characterization. Phase noise is TYPICAL value at 25°C.
9. With stated inductance values, muRata LQW18, on reference test board. Other frequency ranges may be obtained using different inductor values. With accurate design of the PCB and selection of the inductors, VCO frequencies up to about 1.9GHz (RF) and 500MHz (IF) can be obtained. Please refer to the data sheet [RD1], Section 13.3.6, for VCO alignment and PCB design requirements.
10. OIx and OQx shall NOT be loaded with less than 10kΩ, otherwise severe signal distortion and amplitude limiting (clipping) will occur.

2.7 Parameter Drift Values

See reference [RD5].

2.8 Intermediate and End-point Electrical Measurements

The intermediate and end-point measurements have been performed at:

T_{amb} = +25 ± 1°C

for the supply voltages:

2.4V, 3.0V and 3.6V

2.9 Burn-in Conditions

The burn-in condition test follows MIL-STD-883 method 1015:

Condition T = 125°C for 240h

2.10 Operating Life Conditions

The temperature cycling test follows MIL-STD-883 method 1015:

T = 125°C, t = 2000h

3 DESCRIPTION OF THE CHANGES

3.1 Changes from 1-V to 1-W

Reason: re-characterization of the SY1007, corrected inconsistencies (request from a customer).

- Ported document to Open Document Format (ISO/IEC 26300-1:2015).
- Added disclaimer and copyright notice on page 2.
- Updated reference documents (Table 1) to newest versions available.
- Updated RF-VCO tuning range and sensitivity (4.7nH inductor).
- Updated IF-VCO tuning range and sensitivity – range adjusted in dependence on the inductor value (customer specific).
- Corrected IF-PLL main divider range – typo in range corrected.
- Pin-out: corrected inconsistency, I and Q outputs were swapped in Table 5.
- Refinement/improvement of many specs (improved phase noise, spurs, timing).
- Several editorial changes, correction of typos, new figures (no factual changes).

3.2 Changes from 1-W to 1-X

Reason: added notes in Section 2.6 (requests from customers), corrected minor typos.

- Removed minor pin naming inconsistencies in Table 5, aligned names with data sheet.
- Added notice in Section 2.6, page 20: reference to data sheet and disclaimer.
- Added Notes 9 (VCOs) and 10 (I/Q outputs) under Table 14, similar to data sheet.
- Minor editorial changes, removed redundancy in Section 1.6.

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