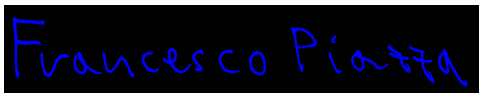
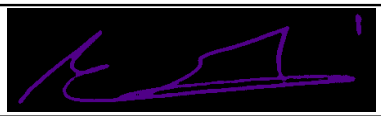
Qualification of the Saphyrion's SY1017CS device

SY1017CS Detailed Specification

Saphyrion Designation: **SY1017CS**

Manufacturer Cross Reference: **----**

Manufacturer: **Saphyrion Sagl**

Signature Field			
Prepared by	*F. Piazza* 	***Date***	*26 May 2015*
Approved by	*A. Consoli* 	***Date***	*26 May 2015*

CHANGE RECORD

Issue/ Revision	Date	Page	Description of Change
1-A	18.07.2007	all	Document creation.
1-B	18.08.2007	all	Document extended.
1-C	25.10.2007	all	Document extended.
1-D	21.11.2007	all	Document updated and extended.
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1-F	10.12.2007	all	Document updated and extended.
1-G	23.09.2008	all	Document updated and extended to be consistent with the values in the test specification.
1-H	23.03.2009	all	Document updated and extended.
1-I	02.06.2009	all	Changed from Nemerix to Saphyrion.
1-L	01.09.2009	all	Updated limits to end of life expected values.
1-M	17.03.2012	all	Updated all sections, changed document format.
1-N	03.04.2012	all	Small refinements.
1-O	20.05.2012	all	Small refinements.
1-P	13.08.2012	all	Small refinements based on July 2012 review.
1-Q	21.09.2012	all	Small refinements based on August 2012 reviews.
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1-S	12.02.2013	all	Small refinements based on February 2013 review.
1-T	18.02.2013	all	Small modifications according to 14th February 2013 e-mail (YZ).
1-U	06.03.2013	16-19	Corrected typos in figures 2.1 and 2.2 and in table 2.4.
1-V	12.03.2013	1	Updated signature field on front page. Changed note 5 of table 2.6.
1-W	26.05.2015	all	Re-characterization of the SY1017C, updated all sections and tables.

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1 GENERAL

1.1 Scope

This specification details the ratings, physical and electrical characteristics, test and inspection data for the SY1017CS GNSS AD/DA converter and PLL IC processed on Si/Ge technology. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification 9000.

1.2 Applicable Documents

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 Reference Documents

RD	Title	Version	Date
1	Saphyrion Sagl *SY1017C AD/DA-Converter, PLL Datasheet*	1.5	30.01.2014
2	Saphyrion Sagl *SY1017/17C Test Specification*	2.2	13.09.2012
3	Micross (TS2-micro) *Process Identification Document - PID106*	6	26.06.2012
4	Optocap *Process Identification Document*		26.06.2012
5	Saphyrion Sagl *G3 ASIC Lot Validation 2 SY1017CS Drift Analysis report*	1-B	14.01.2013

Table 1: Reference documents.

1.4 Terms, Definitions, Abbreviations, Symbols and Units

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.5 Component Number and Component Type Variants

1.5.1 Component Number

The component type number shall be constituted as follows:

SY1017CS

1.5.2 Marking

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall as a minimum be:

(a) Terminal identification.
(b) Component number.
(c) Traceability information.

← A1 dot and die part number: 17C=SY1017C.
← YYWW = Year and week of sealing.
← S = FM part, xxx = Unique serial number.

Marking	Meaning
Dot	Pin A1 position
17C	Part number: SY1017C
YYWW	Year and week of sealing
S	FM part
xxx	Unique serial number

Table 2: Marking on chip and meaning.

1.5.3 Component Type Variants

The component type variants applicable to this specification are as follows.

Variant number	Based on type	Circuit function	Analogue supply voltage	Digital supply voltage	Case	Terminal material and finish	Weight max
01	SY1017CS	AD/DA Converter, PLL	2.4V to 3.6V	2.2V to 3.6V	BGA-36	60/40 SnPb solder balls over Ni/Au plating	0.2g

Table 3: Component type variants.

Notes:

- Nickel: 2µm < Ni thickness < 8µm.
- Gold: Au removed before ball attachment.

1.6 Absolute Maximum Ratings

The absolute maximum ratings shall not be exceeded at any time during use or storage. Absolute maximum ratings shall only be exceeded during testing to the extent specified in this specification.

Absolute maximum ratings are short term stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Characteristic	Symbol	Maximum rating	Unit	Notes
Positive analogue supply voltage	AVDD	4.0	V	1
Positive digital supply voltage	DVDD	4.0	V	1
ESD susceptibility, HBM, JESD22-A114	V(HBM)	Class 1B, 1	kV	
Continuous power dissipation	P	300	mW	2
Current on any input (analogue and digital) and LF		±1	mA	3
Current on any output and I/O (analogue and digital) except LF		±10	mA	
Current on analogue supply pins		±10	mA	
Current on digital supply pins		±50	mA	
Voltage on any pin	Vmax	-0.3 / xVDD+0.3	V	4
Operating junction temperature, guaranteed performance	Top	-40 to +125	°C	5
Operating junction temperature, no degradation	Tnd	-55 to +125	°C	6
Storage Temperature	Tst	-65 to +150	°C	
Soldering Temperature	Tsol	240	°C	7

Table 4: Absolute maximum ratings.

Notes:

1. From AVDD to AVSS, from DVDD to DVSS. MAX DC voltage between AVSS and DVSS ≤ ±100mV.
2. Provided maximum junction temperature is not exceeded.
3. Any pin except power supply.
4. Provided other maximum ratings are not exceeded.
5. With specified performance.
6. Functional performance is not guaranteed outside $T_{op.}$
7. Duration 40 seconds maximum.

1.7 Handling Precautions

ESD sensitive devices: these devices are susceptible to damage by electrostatic discharge, therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, packaging, shipment and any handling.

These components are categorized as Class 1B with a minimum critical path failure voltage of 1000V HBM when tested in accordance with JESD22-A114.

1.8 Functional Description

The SY1017CS is a radiation hardened AD/DA-converter and interface ASIC for GNSS receivers aimed at aerospace applications. It is designed to operate together with the SY1007S GNSS RF front-end and its purpose is to interface it to a GNSS baseband processor. The SY1017CS integrates two flash AD-converters, a low speed DA-converter, a sampling clock PLL frequency synthesizer and a configuration register accessible via a serial interface. It directly interfaces to the ESA AGGA-4 GNSS base-band processor.

The SY1017CS is implemented in a 0.35µm SiGe HBT process and comes in a ceramic-metal hermetic 36 balls CBGA package containing no organic materials, while eutectic – rather than epoxy – die attach has been used. This device will therefore not decompose or release any substantial amount of gas or organic contaminants under vacuum or high radiation levels.

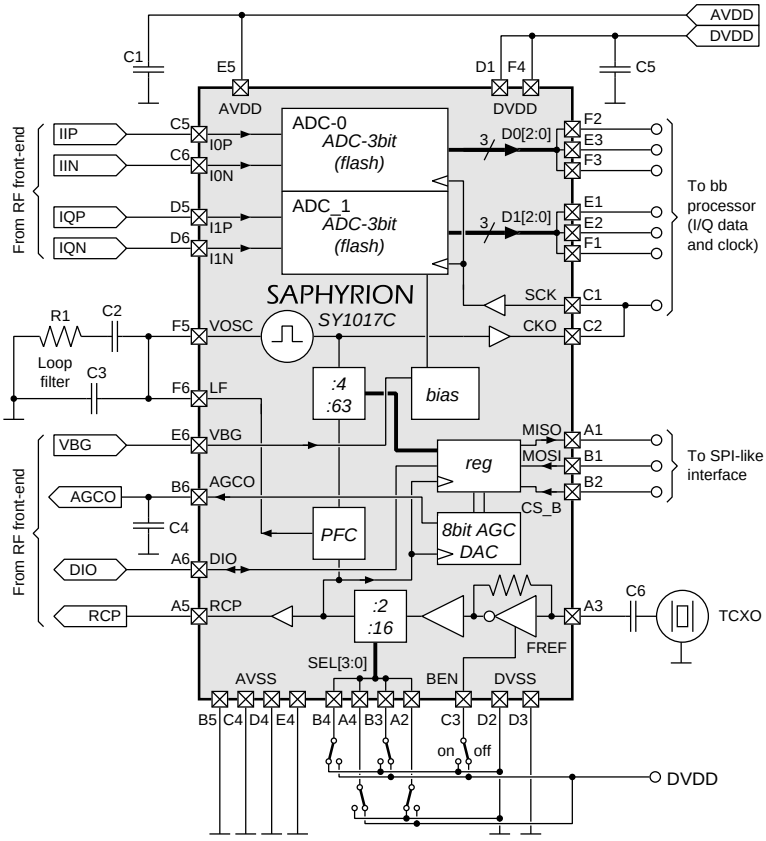

Figure 1: SY1017CS functional diagram.

1.9 Physical Dimensions

The CBGA package of the SY1017CS is of ceramic-metal hermetic design, similar in shape to a plastic BGA, JEDEC MO-216, variant BAA-2 (thickness is larger). Connection to the PCB is via solder balls, which result in a rather rigid assembly.

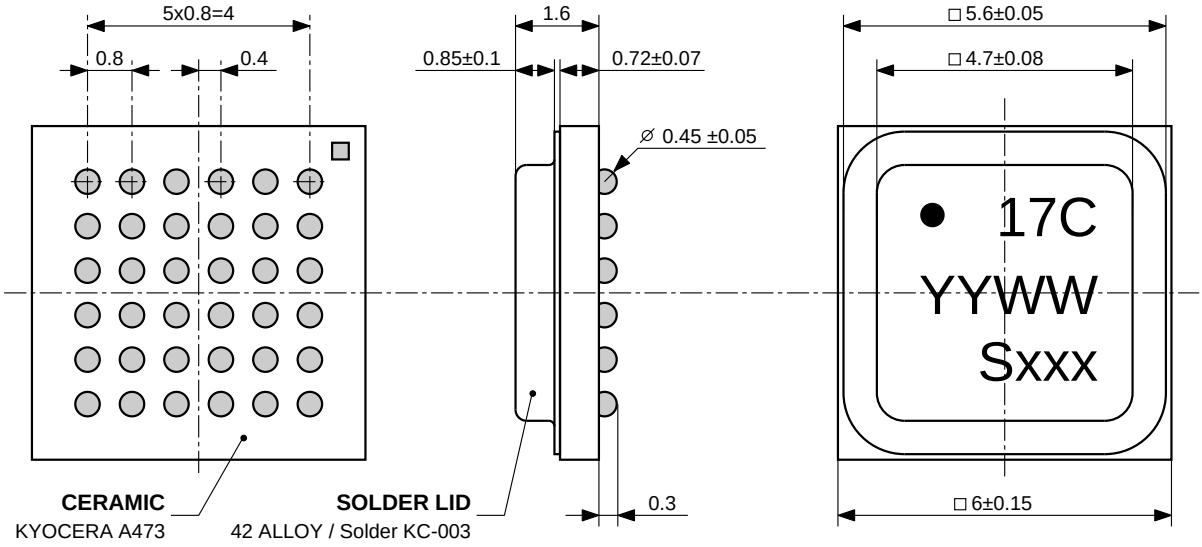

Figure 2: SY1017CS mechanical drawing (CBGA 36 balls).

1.10 Pin Identification

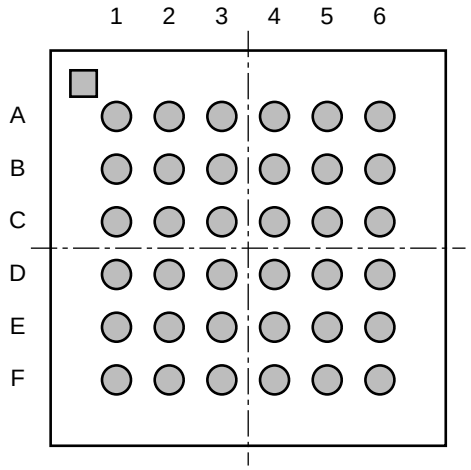

Figure 3: SY1017CS pin-out (top view).

Name	Ball	Function	Notes
		A-balls	
MISO	A1	Serial interface: master in slave out, scan out.	
SEL[0]	A2	Reference divider, bit 0, test enable.	
FREF	A3	TCXO/OCXO clock input.	1Vpp clipped sine or full swing digital.
SEL[2]	A4	Reference divider, bit 2, test enable.	
RCP	A5	Reference clock for PLL and serial interface.	
DIO	A6	Single wire interface for SY1007S.	Needs a weak pull-down.
		B-balls	
MOSI	B1	Serial interface: master out slave in, scan input.	
CS_B	B2	Serial interface: chip select, scan enable.	
SEL[1]	B3	Reference divider, bit 1, test enable.	
SEL[3]	B4	Reference divider, bit 3, test enable.	
AVSS	B5	Negative analogue supply voltage.	
AGCO	B6	8-bit AGC DA-converter output.	
		C-balls	
SCK	C1	AD-converter's sampling clock input.	
CKO	C2	PLL frequency synthesizer output.	Independent from SCK.
BEN	C3	TCXO/OCXO buffer enable.	Active low.
AVSS	C4	Negative analogue supply voltage.	
I0P	C5	First AD-converter positive input.	
I0N	C6	First AD-converter negative input.	
		D-balls	
DVDD	D1	Positive digital supply voltage.	Decouple to DVSS close to the chip.
DVSS	D2	Negative digital supply voltage.	
DVSS	D3	Negative digital supply voltage.	
AVSS	D4	Negative analogue supply voltage.	
I1P	D5	Second AD-converter positive input.	
I1N	D6	Second AD-converter negative input.	
		E-balls	
D1[2]	E1	Second AD-converter digital output: bit 2.	
D1[1]	E2	Second AD-converter digital output: bit 1.	
D0[1]	E3	First AD-converter digital output: bit 1.	
AVSS	E4	Negative analogue supply voltage.	
AVDD	E5	Positive analogue supply voltage.	Decouple to AVSS close to the chip.
VBG	E6	1.2V voltage reference input.	Required, device has no on-chip ref.
		F-balls	
D1[0]	F1	Second AD-converter digital output: bit 0.	
D0[2]	F2	First AD-converter digital output: bit 2.	
D0[0]	F3	First AD-converter digital output: bit 0.	
DVDD	F4	Positive digital supply voltage.	Decouple to DVSS close to the chip.
VOSC	F5	VCO control voltage input.	
LF	F6	PLL charge pump output.	

Table 5: Pin-out list.

1.11 Timing Diagram, Data Structure and Register Map

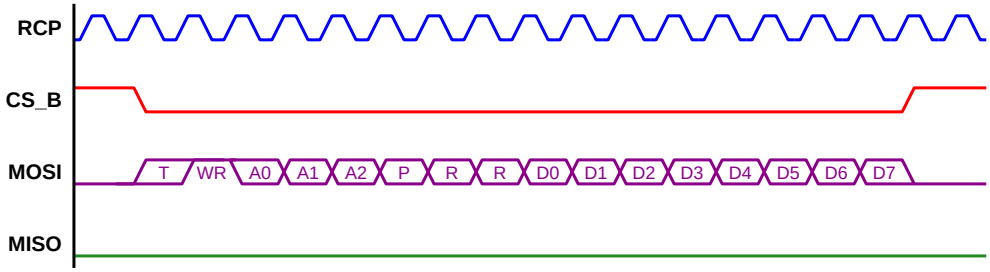

Figure 4: Serial interface write packet.

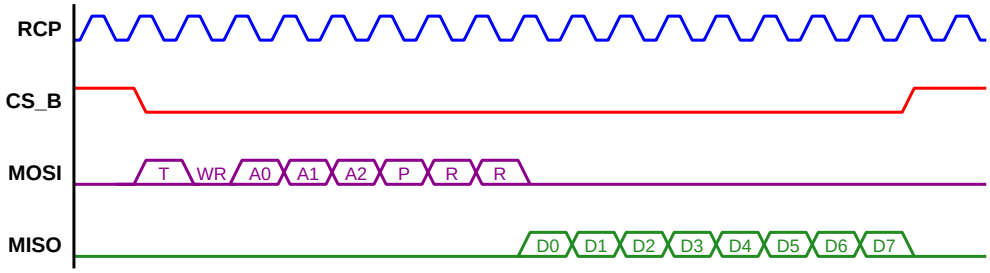

Figure 5: Serial interface read packet.

Field name	Target	Write	Addr [0:2]	Parity	Reserved	Data [0:7]
Position	0	1	2:4	5	6(7)	8:15

Table 6: Data structure.

Fields	**Description**
Target	Determines the physical location of the register being addressed. 0 Register is on SY1017CS device. 1 Register is on SY1007S device.
Read/Write	Transfer direction. 0: Read operation. 1: Write operation.
Addr[0:2]	Register address, LSB-first.
Parity	Parity is calculated on Target, Write and Address fields. Parity is ODD.
Reserved	Reserved, currently unused.
Data[0:7]	Data byte to be written to/read from the interface, LSB-first. Write: Master sends data to be written in register. Read: SY1017CS returns register's content.

Table 7: Structure of the control word.

Target	RW	Register address			Device	Direction	Register Name
		A0	A1	A2			
0	0	0	0	0	SY1017CS	R	(SEU protection)
0	0	0	0	1	SY1017CS	R	Power Modes / PLL
0	0	0	1	0	SY1017CS	R	AGC-DAC
0	0	0	1	1	SY1017CS	R	Reserved
0	0	1	0	0	SY1017CS	R	Reserved
0	0	1	0	1	SY1017CS	R	Reserved
0	0	1	1	0	SY1017CS	R	Reserved
0	0	1	1	1	SY1017CS	R	Reserved
0	1	0	0	0	SY1017CS	W	(SEU protection)
0	1	0	0	1	SY1017CS	W	Power Modes / PLL
0	1	0	1	0	SY1017CS	W	AGC-DAC
0	1	0	1	1	SY1017CS	W	Reserved
0	1	1	0	0	SY1017CS	W	Reserved
0	1	1	0	1	SY1017CS	W	Reserved
0	1	1	1	0	SY1017CS	W	Reserved
0	1	1	1	1	SY1017CS	W	Reserved
1	0	0	0	0	SY1007S	R	RF-PLL
1	0	0	0	1	SY1007S	R	Reserved
1	0	0	1	0	SY1007S	R	Power Modes
1	0	0	1	1	SY1007S	R	Reserved
1	0	1	0	0	SY1007S	R	IF-PLL
1	0	1	0	1	SY1007S	R	Reserved
1	0	1	1	0	SY1007S	R	Reserved
1	0	1	1	1	SY1007S	R	Reserved
1	1	0	0	0	SY1007S	W	RF-PLL
1	1	0	0	1	SY1007S	W	Reserved
1	1	0	1	0	SY1007S	W	Power Modes
1	1	0	1	1	SY1007S	W	Reserved
1	1	1	0	0	SY1007S	W	IF-PLL
1	1	1	0	1	SY1007S	W	Reserved
1	1	1	1	0	SY1007S	W	Reserved
1	1	1	1	1	SY1007S	W	Reserved

Table 8: Register's map.

Notes:

1. Reserved locations are ignored. They should not be accessed to maintain compatibility with future extensions.
2. SEU protection is a dummy register that is always ignored. If a SEU causes a false write, no register corruption will result.

1.12 ESD Protection Networks

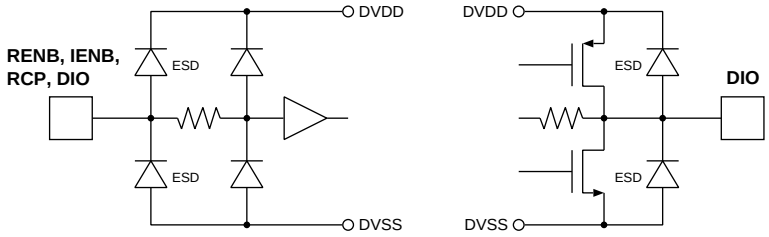

Figure 6: Digital inputs and outputs.

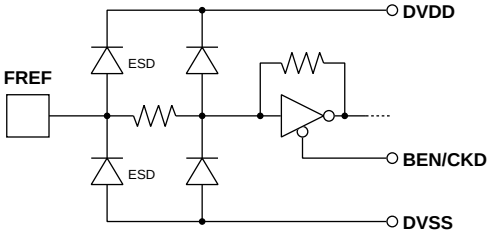

Figure 7: TCXO/OCXO clock input.

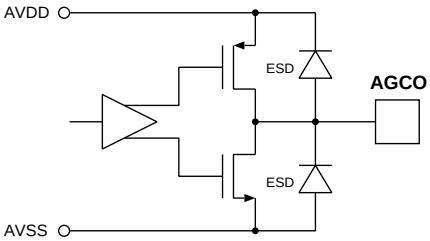

Figure 8: 8-bit AGC DA-converter output.

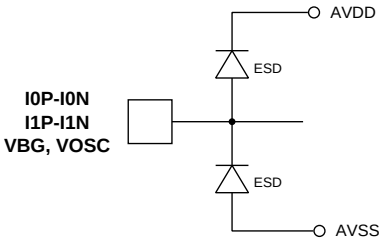

Figure 9: Analogue input pins.

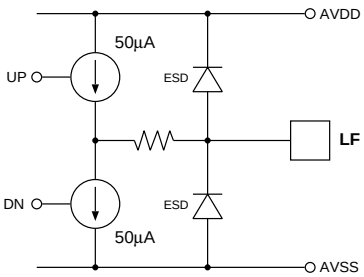

Figure 10: PLL charge pump output.

2 REQUIREMENTS

2.1 General

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are as listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from Screening Tests – Chart F3

High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB Burn-in shall be omitted.

2.2 Wafer Manufacturing & Preparation

For 3 wafers B4681 manufactured at AMS the wafer lot acceptance data are prepared according to ESCC9000 Chart F2 – Production Control – Wafer Lot Acceptance. The Wafer Lot Acceptance data consists of the Process Monitoring Review supported by the Process Identification Document (PID), the SEM Inspection and the Total Dose Radiation Testing (TID). During the development of the SY1017CS TID and Single Event Effects (SEE) testing have been performed, only the TID testing is repeated for the flight wafer.

Test type	Specification	SY1017CS
Process Monitoring Review	ESCC9000, Chart F2	
SEM Inspection	ESCC9000, Chart F2	4 pieces per wafer
TID Testing	ESCC9000, Chart F2	4 pieces

Table 9: Wafer lot acceptance.

2.3 Production of Flight Lot

During this activity the parts for the flight lot are packaged according to ESCC9000 Chart F2 – Production Control – Special In-Process Controls.

The following steps are performed:

- Die assembly.
- Pre-cap inspection.
- Sealing.
- Marking of the devices.
- Balling.

Test type	Specification	SY1017CS
Internal visual inspection	ESCC9000, Chart F2	All
Pre-cap inspection – Low magnification – High magnification	ESCC9000, Chart F2	 All 50 pieces
Bond strength at pre-cap	ESCC9000, Chart F2	3 pieces
Die shear at pre-cap	ESCC9000, Chart F2	3 pieces
External dimension check at pre-cap	ESCC9000, Chart F2	3 pieces
Co-planarity of solder balls	ESCC9000, Chart F2 Co planarity (CO) < 120µm	All

Table 10: Special in-process controls.

2.4 Screening of Flight Lot

During this activity the parts for the flight lot are screened according to ESCC9000 Chart F3 (Figure 11). The tests are given in Table 11.

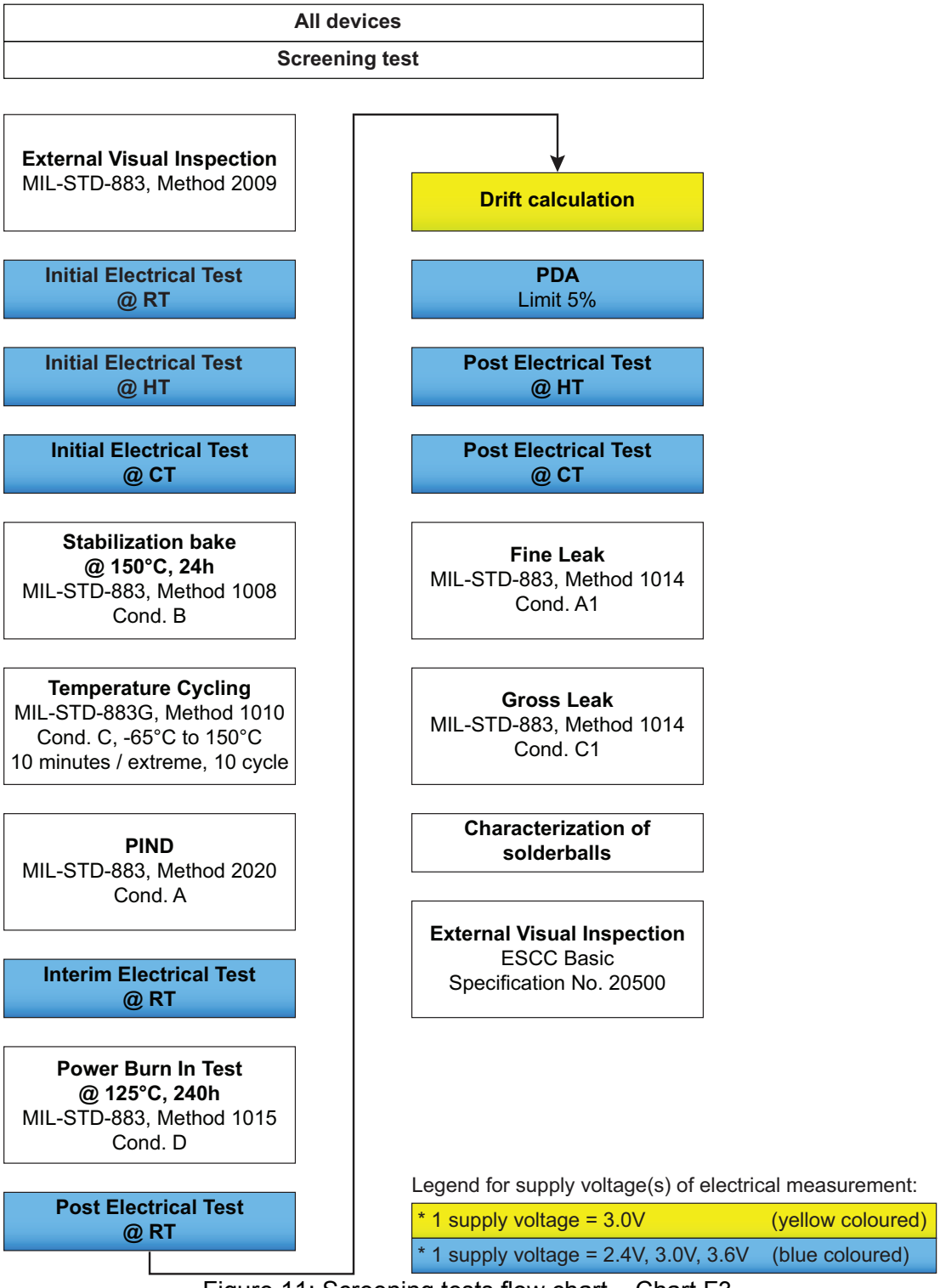

Figure 11: Screening tests flow chart – Chart F3.

Test type	Specification	SY1017CS
Initial electrical test room temperature	ESCC9000, Chart F3 SY1017CS-Test Spec, chapter 6	All
Initial electrical test high temperature	ESCC9000, Chart F3 SY1017CS-Test Spec, chapter 6	All
Initial electrical test cold temperature	ESCC9000, Chart F3 SY1017CS-Test Spec, chapter 6	All
150°C temperature stabilisation bake for 24h	ESCC9000, Chart F3	All
Temperature cycling form -65°C to 150°C, 10 minutes for 10 cycles	ESCC9000, Chart F3	All
Particle impact noise detection (PIND)	ESCC9000, Chart F3	All
Interim electrical measurements at room temperature	ESCC9000, Chart F3 SY1017CS-Test Spec, chapter 7	All
Power burn-in under nitrogen atmosphere	ESCC9000, Chart F3	All
Post electrical measurements at room temperature	ESCC9000, Chart F3 SY1017CS-Test Spec, chapter 7	All
Drift calculation	ESCC9000, Chart F3 SY1017CS-Test Spec, chapter 7	
PDA limits (5%)		
Characterization of solder balls (optical, co-planarity)	ESCC9000, Chart F3, **note 1**	All
Seal (fine and gross leak)	ESCC9000, Chart F3	All
External visual inspection	ESCC9000, Chart F3	All
Check for lot failure	ESCC9000, Chart F3	All

Table 11: Screening tests.

Notes:

1. Visual inspection of solder balls. Criteria: no missing balls, no missing material of the surface and co-planarity shall be less than 0.12mm (120µm).

2.5 Lot Validation of Flight Lot

During this activity a set of reliability tests is performed on the packaged parts. The tests and the number of samples are given in Table 12, whereas the test flow is provided in Figure 12.

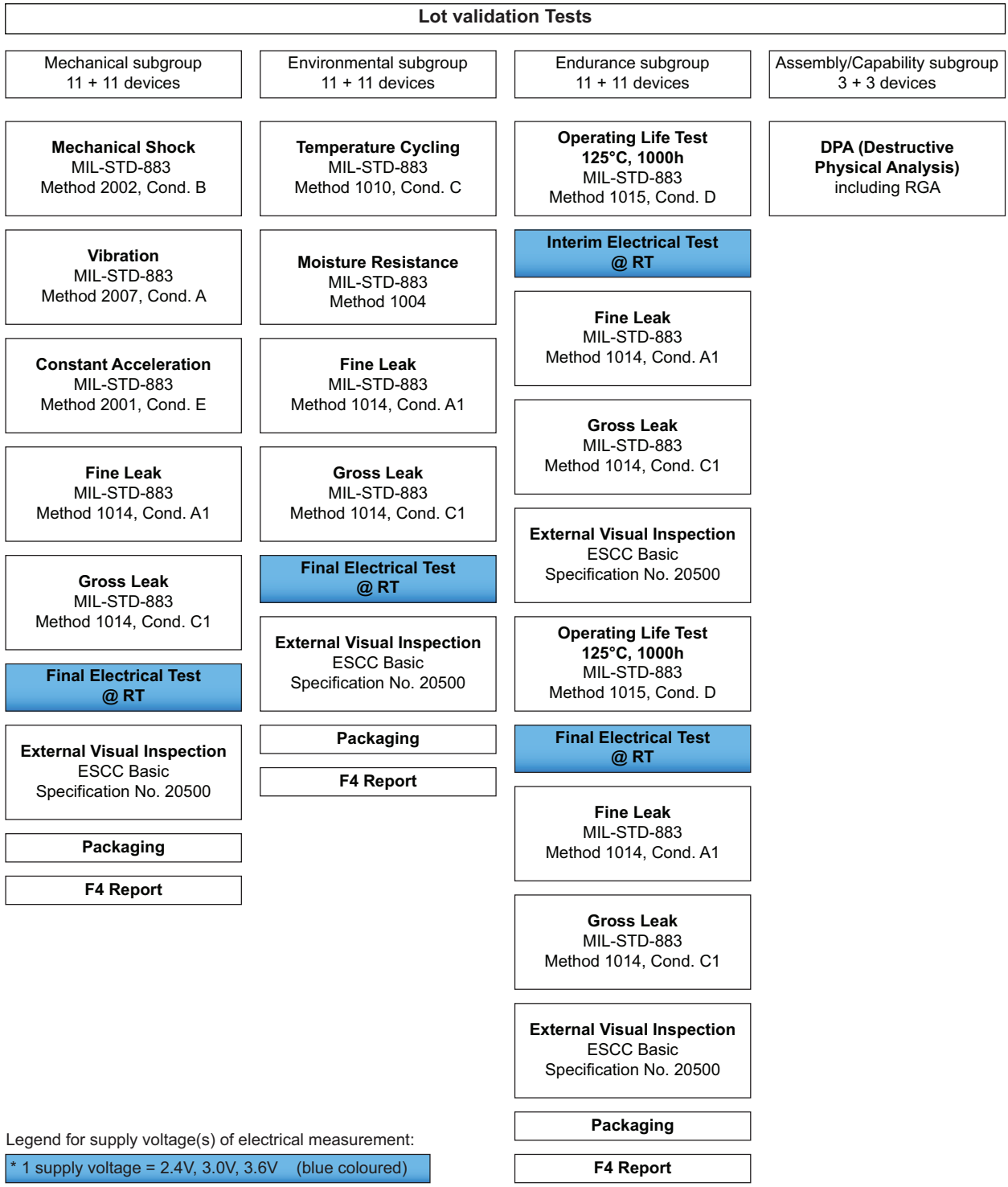

Figure 12: Qualification and periodic tests flow chart – Chart F4.

Test type	Specification	SY1017CS
Solderability	TP-PLN-0036-AAE_	5 pieces
F4-Qualification Tests – Mechanical Subgroup		11 pieces
Mechanical shock	ESCC9000, Chart F4, Subgroup 1	11 pieces
Vibration	ESCC9000, Chart F4, Subgroup 1	11 pieces
Constant acceleration	ESCC9000, Chart F4, Subgroup 1	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
Final electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 1 SY1017CS -Test Spec, chapter 7	11 pieces
F4-Qualification Tests – Environmental Subgroup		11 pieces
Temperature cycling (10 cycles)	ESCC9000, Chart F4, note 1	11 pieces
Moisture resistance	ESCC9000, Chart F4, Subgroup 1	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
Final electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 1 SY1017CS-Test Spec, chapter 7	11 pieces
F4-Qualification Tests – Endurance Subgroup		11 pieces
Operating Life test on qualification sample 1000h	ESCC9000, Chart F4, Subgroup 2	11 pieces
Interim electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 2 SY1017CS-Test Spec, chapter 7	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
External visual inspection	ESCC9000, Chart F4, Subgroup 1	11 pieces
Operating life test on qualification sample 1000h	ESCC9000, Chart F4, Subgroup 2	11 pieces
Final electrical test (room temperature)	ESCC9000, Chart F4, Subgroup 2 SY1017CS-Test Spec, chapter 7	11 pieces
Seal (fine and gross leak)	ESCC9000, Chart F4, Subgroup 1	11 pieces
External visual inspection	ESCC9000, Chart F4, Subgroup 1	11 pieces
F4-Qualification Tests – Assembly/Capability Subgroup		3 pieces
External visual inspection	ESA/SCC Basic Specification No. 2059000, Issue 1, September 1994.	3 pieces
Radiographic inspection	ESA/SCC Basic Specification No. 2099000, Issue 1, September 1994.	3 pieces
PIND test	MIL-STD-883, Method 2020, Cond. A.	3 pieces
Hermetic seal tests	MIL-STD-883, Method 1014, Cond. A1 and C1.	3 pieces
Internal gas analysis	MIL-STD-883, Method 1018.	3 pieces
Internal visual inspection	ESCC Basic Specification No. 2049000, Issue 2, November 2003.	3 pieces
Bond strength	MIL-STD-883, Method 2011.	3 pieces
Die shear strength	MIL-STD-883, Method 2019.	3 pieces

Table 12: Lot validation tests and number of samples.

Notes:

1. The temperature cycling (MIL-STD-883, Method 1010, Condition C) present in the test flow is defined in the ESCC9000, issue 1 (October 2002) and older version as part of the flow. At the time of the qualification of the lot 1 this was the version in use and temperature cycling was agreed with ESA and RUAG as enough. Because of that, the thermal shock was not implemented as part of the flow.

2.6 Electrical Measurements at Room, High and Low Temperatures

Conditions: AVDD = 2.4V to 3.6V, DVDD = 2.2V to AVDD + 0.2V, Tjunction = −40°C to +125°C, no load, unless otherwise stated. All voltages are referred to their respective VSS. Typical values are at AVDD = 3.0V, DVDD = 3.0V, Tjunction = +25°C.

Characteristics	Symbol	Test Conditions	Limits		Unit	Ref. to [RD2]	Notes
			Min	Max			
Power supply							
Analogue supply current	I_{SSA}	Sleep	0.0	8.0	µA	6.4.1	1
		PLL Active	140	415	µA	6.4.2	1
		ADC DAC active	1.6	2.4	mA	6.4.3	1
Digital supply current	I_{SSD}	Sleep, leakages	0.0	8.0	µA	6.4.1	1
		Sleep. TCXO buffer bias current	5	72	µA	6.4.1	1
		PLL Active	3.0	8.0	mA	6.4.2	1
		ADC DAC active	40	120	µA	6.4.3	1
Digital section							
Digital output high level	VDOH	IOH = -1mA	0.9X DVDD		V	6.5.1	1
Digital output low level	VDOL	IOL = 1mA		0.1X DVDD	V	6.5.1	1
Digital output rise time	t_{rise}	c_{load} = 5pF		4.9	ns		2
Digital output fall time	t_{fall}	c_{load} = 5pF		3.8	ns		2
Reference clock							
FREF input level AC coupled	$Fref_{ac}$	Sine wave. Input must be AC coupled.	0.4		Vpp	6.3	1
FREF input level DC coupled	$Fref_{DCL}$	Square wave VIL (BEN=VIL)	−0.2	0.3x DVDD	V	5.7	1
	$Fref_{DCH}$	Square wave VIH (BEN=VIL)	0.7x DVDD	DVDD +0.2	V	5.7	1
External reference clock	RCP	SY1017CS ⎵ BEN = 1 FREF = 32MHz SEL[3:0]				6.5.2	1
		0001	15.52	16.48	MHz		
		0010	10.35	10.99	MHz		
		0011	7.76	8.24	MHz		
		0100	6.21	6.59	MHz		
		0101	5.17	5.49	MHz		
		0110	4.34	4.71	MHz		
		0111	3.88	4.12	MHz		
		1000	3.45	3.66	MHz		
		1001	3.10	3.30	MHz		
		1010	2.82	3.00	MHz		
		1011	2.59	2.75	MHz		
		1100	2.39	2.54	MHz		
		1101	2.22	2.35	MHz		
		1110	2.07	2.20	MHz		
		1111	1.94	2.06	MHz		
TCXO buffer current	I_{tcxo}	BEN = 0 → Buffer off	−5	5	µA	6.5.3	1
TCXO buffer DC bias	V_{tcxo}	BEN = 1 → Buffer on	0.5	0.9	V	6.5.3	1
PLL frequency synthesizer							
PLL PFC voltage swing	VS_{LF}	On LF	0.7	2.2	V	6.5.4	1
PLL VCO frequency range	f_{PLL}		20	50	MHz	6.5.4	1
PLL VCO sensitivity	Sens		60	130	MHz/V		3
PLL PFC gain	PLL_{gain}		6.7	9.55	µA/rad		3
PLL PFC output current	IO_{PLL}		40	60	µA		3

Characteristics	Symbol	Test Conditions	Limits		Unit	Ref. to [RD2]	Notes
			Min	Max			
PLL SSB phase noise	φn	100Hz offset		−65	dBc/Hz		7
		1kHz offset		−65	dBc/Hz		7
		10kHz offset		−58	dBc/Hz		7
		100kHz offset		−60	dBc/Hz		7
		1MHz offset		−88	dBc/Hz		7
		10MHz offset		−112	dBc/Hz		7
PLL spurs		Recommended loop filter		−40	dBc		7
AD-converter							
ADC input bias voltage	V_{inDC}		570	630	mV	6.5.5	1
ADC output codes vs input voltage	Vth	P +250mV N +950mV	000			6.5.5	1
		P +350mV N +850mV	001			6.5.5	1
		P +450mV N +750mV	010			6.5.5	1
		P +550mV N +650mV	011			6.5.5	1
		P +650mV N +550mV	100			6.5.5	1
		P +750mV N +450mV	101			6.5.5	1
		P +850mV N +350mV	110			6.5.5	1
		P +950mV N +250mV	111			6.5.5	1
ADC differential non-linearity	DNL_{ADC}		−1	1	LSB	6.5.5	1
ADC integral non-linearity	INL_{ADC}		−1	1	LSB	6.5.5	1
ADC differential input resistance	Rdif		32	48	kΩ		3, 4
ADC Input Bandwidth	BW_{ADC}	FS, Sine, -3dB.	25	60	MHz		3
ADC resolution	Res	No missing codes.		3	Bit		1
ADC DC offset error	DC-OS		−50	50	mV		3
ADC gain error	ΔG		−10	10	%FSR		3, 5
ADC aperture time	t(ap)			2	ns		3
DA-converter							
DAC output voltage	V(AGCO)		0.2	2.2	V	6.5.6	1
DAC gain	Gain		6.5	9.0	mV/LSB	6.5.6	1
DAC gain error	DAC_{gain}		−5	5	%FSR		3, 6
DAC gain error drift	DAC_{drift}	Over temperature.	−5	5	%FSR		3, 6
DAC differential non-linearity	DNL_{DAC}		−4	4	LSB	6.5.6	1
DAC integral non-linearity	INL_{DAC}		−4	4	LSB	6.5.6	1
DAC bandwidth	BW_{DAC}	FS, Sine, −3dB.	1		kHz		3
DAC output current	IO_{DAC}			100	µA		3
DAC output impedance	Z_{DAC}			10	Ω		3
VBG input impedance	Z_{vbg}		80	160	kΩ		3

Table 13: Functional tests independent from temperature.

Notes:

1. Fully tested over temperatures −40°C, 25°C, 125°C, and voltages 2.4V, 3.0V, 3.6V. Selected parameters are tested at limits different than shown in the data sheet, either to get margin (tighter limits) or to account for the non-ideal test system (looser limits). Current consumption in Sleep mode is masked by tester resolution and leakages. Typical current consumption in Sleep mode is <100nA on both AVDD and DVDD (also at 125°C).
2. As 1 but calculated from measurement at higher load capacitances (load board stray and tester input capacitance are >> 15pF).
3. Not production tested, guaranteed by design over temperature of −40°C to +125°C.
4. Coupling capacitors are needed. ADC is internally biased.
5. Referred to VBG. Gain error is uncritical as long as maximum limit of $800mV_{pp}$ is not exceeded. The SY1007, which generates the VBG voltage, is designed not to exceed the above required limit under all conditions.
6. Referred to VBG. SY1007S AGC must be driven to 2.0V worst case at low temperature. Combined gain error and drift guarantees 2.0V output.
7. Not production tested, only characterization. Phase noise is TYPICAL value at 25°C.

2.7 Parameter Drift Values

See reference [RD5].

2.8 Intermediate and End-point Electrical Measurements

The intermediate and end-point measurements have been performed at T_{amb} = +25 ± 1°C for the supply voltages 2.4V, 3.0V and 3.6V.

2.9 Burn-in Conditions

The burn-in condition test follows MIL-STD-883 method 1015:

Condition T = 125°C for 240h

2.10 Operating Life Conditions

The temperature cycling test follows MIL-STD-883 method 1015:

T = 125°C, t = 2000h

End of document

